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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/739,752	12/20/2000	Vincent Chen	1875.0220000	4979

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EXAMINER

DIAZ, JOSE R

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 06/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application N .

09/739,752

Applicant(s)

CHEN ET AL.

Examiner

José R Díaz

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 April 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 11. 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

➤ A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 11, 2003 has been entered.

### ***Claim Rejections - 35 USC § 102***

➤ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

➤ Claims 1-3, 5-10, 12-18 and 20-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Karp et al. (US Pat. No. 6,266,269 B1).

Regarding claims 1 and 8, Karp et al. teaches a one-time programming memory element comprising: a capacitor (303) having an oxide capable of passing direct gate tunneling current (see Fig. 3A and col. 6, lines 51-53); and a write switch (302) including

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plural transistors each having a gate oxide layer that is thicker than said capacitor oxide layer (see Fig. 3A and 3B and col. 6, lines 30-40); wherein said capacitor is one-time programmable as an anti-fuse by application of a voltage across said capacitor oxide layer via said write switch transistors to cause direct gate tunneling current to rupture said capacitor oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less (see col. 6, lines 50-52).

Regarding claims 2, 9 and 18, Karp et al. teaches that the capacitor oxide layer is approximately 20 Å thick (see col. 6, lines 38-40).

Regarding claims 3 and 10, Karp et al. teaches that the capacitor (303) comprises a FET having source (S) and drain (D) regions coupled to ground, a gate coupled to said switch (302) and a gate dielectric forming said oxide layer (see Fig. 3A and col. 6, lines 46-53).

Regarding claims 5, 12 and 17, Karp et al. teaches that said write switch comprises a 5-volt tolerant switch having a plural 2.5-volt transistors and wherein the voltage is less than 7 volts (see col. 8, lines 58-61).

Regarding claims 6-7 and 13-14, Karp et al. teaches a sensing circuit (141(1), 141(2), 141(3) 141(4), and 343) to sense whether the capacitor is programmed (see Fig. 3B).

Regarding claim 15 and 20, Karp et al. teaches a first switch (302) and a second switch (304) connected to the capacitor (303) (see Fig. 3B)

Regarding claim 16, Karp et al. teaches a read transistor (304), coupled to the capacitor (303), having a gate oxide layer that is thicker than said capacitor oxide layer (see Fig. 3A and 3B and col. 6, lines 30-40).

Regarding claim 21, Karp et al. teaches that the first switch (302) and the second switch (304) have a gate oxide layer that is thicker than said capacitor oxide layer (see Fig. 3A and 3B and col. 6, lines 30-40).

### ***Claim Rejections - 35 USC § 103***

➤ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

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➤ Claims 4, 11 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karp et al. (US Pat. No. 6,266,269 B1) in view of Kim et al. (US 2001/0022746 A1).

Regarding claims 4, 11 and 19, Karp et al. fails to teach a FET having a P-well layer, a deep N-well layer and a P-type substrate. However, Kim et al. teaches that is well known in the art to form a FET having a P-well layer (120) adjacent to the source and drain regions (130A-B), a deep N-well layer (110) below the P-well layer; and a P-type substrate (100) below the deep N-well layer (see Figs. 4A and 6A). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Karp et al. to include an anti-fuse comprising a FET having a P-well layer adjacent to the source and drain regions, a deep N-well layer below the P-well layer; and a P-type substrate below the deep N-well layer. The ordinary artisan would have been motivated to modify Karp et al. in the manner described above for at least the purpose of providing an improved storage cell having a low resistance conductive path.

### ***Response to Arguments***

➤ Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

➤ The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Porter (US Pat. No. 6,351,425 B1) discloses a memory device comprising an anti-fuse (40) (see Figs. 1 and 2); Rao et al. (US Pat. No. 6,549,458 B1)

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discloses a memory element comprising a gate oxide having a thickness of at least 25 Å (see col. 6, lines 60-63); Bell (US Pat. No. 4,173,791) discloses a well-known ROM having a thin gate oxide of 20 Å (see col. 4, lines 19-22); Holmberg et al. (US Pat. No. 4,499,557) discloses a programmable cell (see abstract); and Haeberli et al. (US Pat. No. 6,184,726 B1) discloses a programmable cell (see abstract).

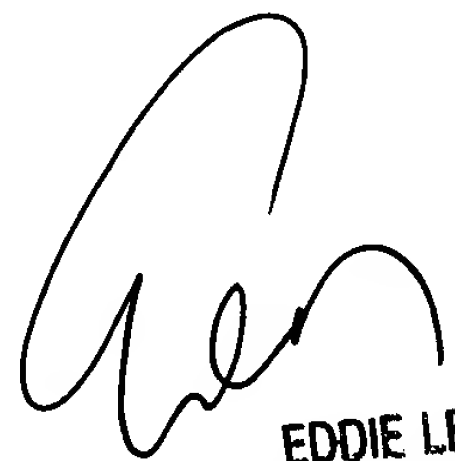
### ***Correspondence***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00-5:00 Monday, Tuesday, Thursday and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 746-3891 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD  
June 18, 2003



EDDIE LEE  
SUPERVISORY PATENT EXAMINER  
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